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# Compact Power BJT and MOSFET models parameter extraction with account for thermal effects

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### **Abstract**

The corrections of the methodology of power BJT and MOSFET transistor models parameter extraction taking into account the self heating effects are presented

For BJT these corrections are included into VBIC model parameter extraction process.

For MOSFET current generator connected to standard SPICE MOS model is proposed to take into account drain current growth with transistor temperature.

### 1. Introduction

Power MOSFET and BJT transistors are widely used in many electronics applications such as DC/DC converters, starter generator systems, automotive applications, UPS invertors, power switches and others. They dissipate large values of power over a small area resulting in very high heat flux so design and simulation of such devices becomes very critical. The failure rate of these devices is a function of their temperature. SPICE simulation for such circuits with account for thermal effects is very important because it gives the possibility to determine transistor temperature depending on its electrical mode. Most specification require that junction temperature be kept below 110°C or even lower to meet the system reliability requirements. The failure rate above this limit increases very rapidly.

Because of strong temperature dependencies of transistor characteristics their correct SPICE simulation becomes more complicated and requires combined electro-thermal simulation [1]. Such a simulation approach results to a more complicated procedure of characteristics measurement and compact model parameter extraction. Unfortunately the procedures for characteristics measurement and

SPICE model parameter extraction with account for the selfheating effects are not described enough.

## 2. Power BJT SPICE model parameter extraction

There are several SPICE models for BJT that can be used for transistor simulation with account for the self heating effects: VBIC [3], MEXTRAM [4], HICUM [5]. MEXTRAM and HICUM models were developed basically for modern high current and high frequency submicron transistors of ICs. As soon as switch power transistors are not deep submicron or very high frequency semiconductor devices, a more simple VBIC model is considered.

It should be mentioned that there have been published a lot of examples of VBIC model application for BJT as IC element but just few publications on VBIC model application for power BJTs.

We illustrated the VBIC model parameter extraction strategy with account for the thermal effects on 828KT2 switch power BJT transistor [6] with the rating parameters, listed in Table 1.

Tabl. 1 Power BJT 828KT2 maximum rating parameters

Symbol	Parameter	Value	Unit
$V_{ce}$	Collector-emitter	50	V
	voltage		
I <sub>c max</sub>	Collector current	15	A
	(peak)		
I <sub>b max</sub>	Base current	6	A
	(peak)		
P <sub>tot</sub>	Total dissipation at	10	W
	$T = -60 + 100^{\circ}C$		

The power BJT model parameter extraction is not a simple process because of a necessity to separate high current and self heating effects. To provide such separation we used the following model parameter extraction sequence.

- 1) VBIC model parameter extraction for normal conditions (room temperature).
  - 2) Temperature effects parameters extraction.
  - 3) Thermal network parameters  $R_{th}$ ,  $C_{th}$  extraction.

To reduce the self heating effect both small and large signal I-V-characteristics were measured using pulse mode [7] with T=23°C

The VBIC model parameters were extracted in the usual way using IC-CAP tool [8] strategy.

The measured and simulated power BJT current gain as a function of collector current and output  $I_c$ =f( $U_{ce}$ ) characteristics at T=23°C are presented in Fig. 1 and 2.

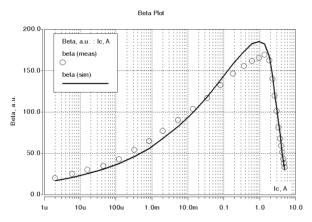


Fig.1. The measured (circles) and simulated (line) current gain of power BJT 828KT2 as a function of collector current (T=23°C).

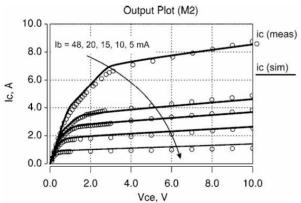


Fig. 2. The measured (circles) and simulated (line) output characteristics of power BJT 828KT2 at 23° C without the selfheating effect.

As a rule circuit designers use default values for temperature effects parameters. The most important one is "xis"- temperature exponent of Is. Unfortunately these defaults value do not provide correct simulation.

Fig. 3 presents comparison of the measured and simulated selfheating characteristics  $\Delta T_{case}, ^{o}C=f(time)$  and  $I_{c}=f(time)$  with default value 3 for "xis" (dotted lines). It is seen that simulation with default temperature parameters evidently underestimates collector current and temperature growth.

To define the model temperature coefficients I-V-characteristics were measured in the temperature range up to 120°C using pulse method and value 4.25 was extracted for "xis".

To extract the thermal network parameters  $R_{th}$ ,  $C_{th}$  the selfheating characteristics ( $I_c \! = \! f(time),$   $T^o \! C \! = \! f(time))$  were measured for transistors without and with different heatsinks using thermocouple and IR methods. The following thermal network parameters were defined for transistor without heatsink:  $R_{th} \! = \! 20$  °C/W,  $C_{th} \! = \! 3.2$  °C/J .

The selfheating  $I_c$ =f(time) and  $T^o$ =f(time) characteristics of power BJT 828KT2 without heatsink simulated with "xis" = 4.25 are presented in Fig. 3 with solid lines.

It is seen that the proposed corrections to VBIC model parameter extraction methodology allows to provide a more correct SPICE simulation with account for selfheating effects.

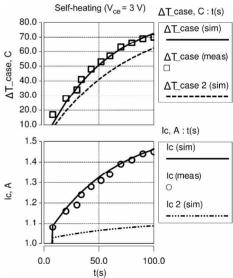


Fig. 3. The measured (circles) and simulated (lines) the selfheating  $\Delta T_{\rm case}$ , °C =f(time) and  $I_{\rm c}$ =f(time) characteristics of power BJT 828KT2 without heatsink. Dotted lines- for default values of temperature coefficients, solid lines- for extracted ones.

# 3. Power MOS FET SPICE model parameter extraction

For purposes of a more accurate SPICE simulation power MOSFETs are represented as macromodel including MOSFET and JFET models and additional elements describing high current and thermal effects [9, 10]. These models in general describe drain current reduction with temperature due to mobility reduction with transistor heating.

Howere in some types of power MOSFETs the working area where drain current  $I_d$  grows with transistor temperature ("thermal runaway") can occupy the main working area [11, 12] that results in necessity of special protection circuits and essentially complicates compact model parameter extraction. This "thermal runaway" area is not always adequately simulated in compact models. We proposed to take into account such anomalous behavior by adding new elements to MOSFET model. As example we considered the power DMOSFET 2P835-A [13] with TO-258 package and the maximum rating parameters, listed in Table 2.

Tabl. 2 Power N-channel DMOSFET 2P835-A [13] maximum rating parameters

maximum rating parameters				
Symbol	Parameter	Value	Unit	
$V_{ m DS}$	Drain-source voltage	100	V	
I <sub>D max cont</sub>	Drain current	50	A	
	(continuous)			
I <sub>D max pulse</sub>	Drain current	100	A	
	(pulsed)			
$P_{tot}$	Total dissipation at	50	W	
	$T = -60100^{\circ}C$			
	(with heatsink)			

Our results of 2P835-A transistor characteristic investigation showed that in addition to drain current growth with transistor temperature (the "thermal runaway" effect) this transistor had the significant drain current growth with drain voltage (see Fig. 4) (with gate voltage above the threshold voltage),

The MOS3 model didn't provide correct  $I_d$ - $V_d$  simulation (see dashed curves in Fig. 4). It was because the MOS3 model described  $I_d$ = $f(V_{ds})$  slope due to threshold voltage reduction with drain voltage in the whole range of gate voltage.

To provide correct simulation of 2P835-A real  $I_d$ = $f(V_{ds})$  characteristics in the wide range of gate and drain voltages, we have modified the standard MOS model (see Fig. 5).

As it is seen, we connected a voltage dependent current source I' in parallel to the standard MOS model. I' referred to MOS3 drain current  $I_d$  as:

$$I' = I_d (1 + K \cdot V_{ds}),$$
where  $K = 0.45$  (for this case).

KP835 Id=f(Vds)

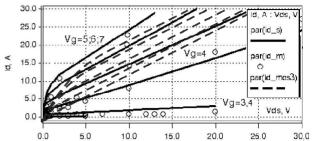


Fig. 4. The measured (circles) and simulated with conventional MOS3 (dashed lines) and modified model (solid lines) output characteristics of power MOSFET 2P835-A without the selfheating effects (T=23°C).

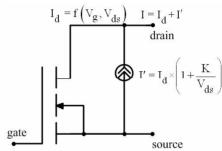


Fig. 5. The modified MOS model describing the temperature dependent drain current growth with drain voltage.

To take into account the drain current growth with transistor temperature T we used the following dependence:

$$I_d = I_d(T_0) \cdot \left(\frac{T}{T_0}\right)^B, \tag{2}$$

where B=0.43 - the fitting parameter,

T - transistor temperature, °C.

 $T_0 = 23$  - reference transistor temperature,  $^{\circ}$ C. Transistor temperature T was calculated using simple a electro-thermal surcircuit (like in [10]) (not shown in Fig. 5).

To separate the self heating and high current effects, the strategy for characteristics measuring and parameter extraction was as the following.

- 1) Standard MOS3 model parameter (for low  $V_{ds}$ ) were extracted using I-V- characteristics measured in the pulse mode.
- 2)  $I_d$ = $f(V_{ds})$  characteristics with high drain voltage and with room temperature were measured in the pulse mode. Macromodel parameter K describing drain current increase with drain voltage was

extracted.

- 3) To define the temperature coefficients for MOS3 model and the macromodel,  $I_d\text{-}V_{ds}$ -characteristics were measured in the temperature range up to  $120^{\circ}\text{C}$  with pulse method.
- 4) The thermal network parameters  $R_{th},\ C_{th}$  were extracted using the selfheating characteristics ( $I_d = f(time),\ T\ ^{o}C\ = f(time))$  for transistors without and with the various heatsinks. For example, the following thermal network parameters were defined for transistor without heatsink:  $R_{th} = 14\ ^{o}C/W,\ C_{th} = 4.6\ ^{o}C/J$  .

The measured and simulated output characteristics of power MOSFET 2P835-A for T=23°C are presented in Fig. 4 and the selfheating drain current characteristics for heatsink mounted transistor are presented in Fig. 6.

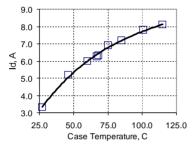


Fig. 6 The measured and simulated the selfheating drain current I<sub>d</sub> dependence on power MOSFET 2P835-A case temperature

### 4. Summary

The corrections of the methodology of power BJT and MOSFET transistor models parameter extraction taking into account the self heating effects are described.

The proposed corrections to VBIC model parameter extraction methodology allowed to provide more correct SPICE simulation with account for selfheating effects in comparison to default model temperature coefficients.

For MOSFET current generator connected in parallel to standard SPICE MOS model allowed to take into account significant drain current growth with drain voltage and with transistor temperature.

The sequence for compact model and macromodel parameter extraction for power transistors included:

- standard I-V-characteristics measuring with room temperature using pulse method and compact model parameter extraction,
- I-V-characteristics measuring with temperature range up to 125°C using pulse method and thermal coefficients parameter extraction,

- selfheating characteristics measuring with and without different heatsinks and thermal network parameters extraction.

The used models and parameter extraction sequence provided SPICE simulation error less than 15% for temperature range from  $20\,^{\circ}\text{C}$  to  $120\,^{\circ}\text{C}$ .

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